Daniel Dreps, et al.
AUS20010742



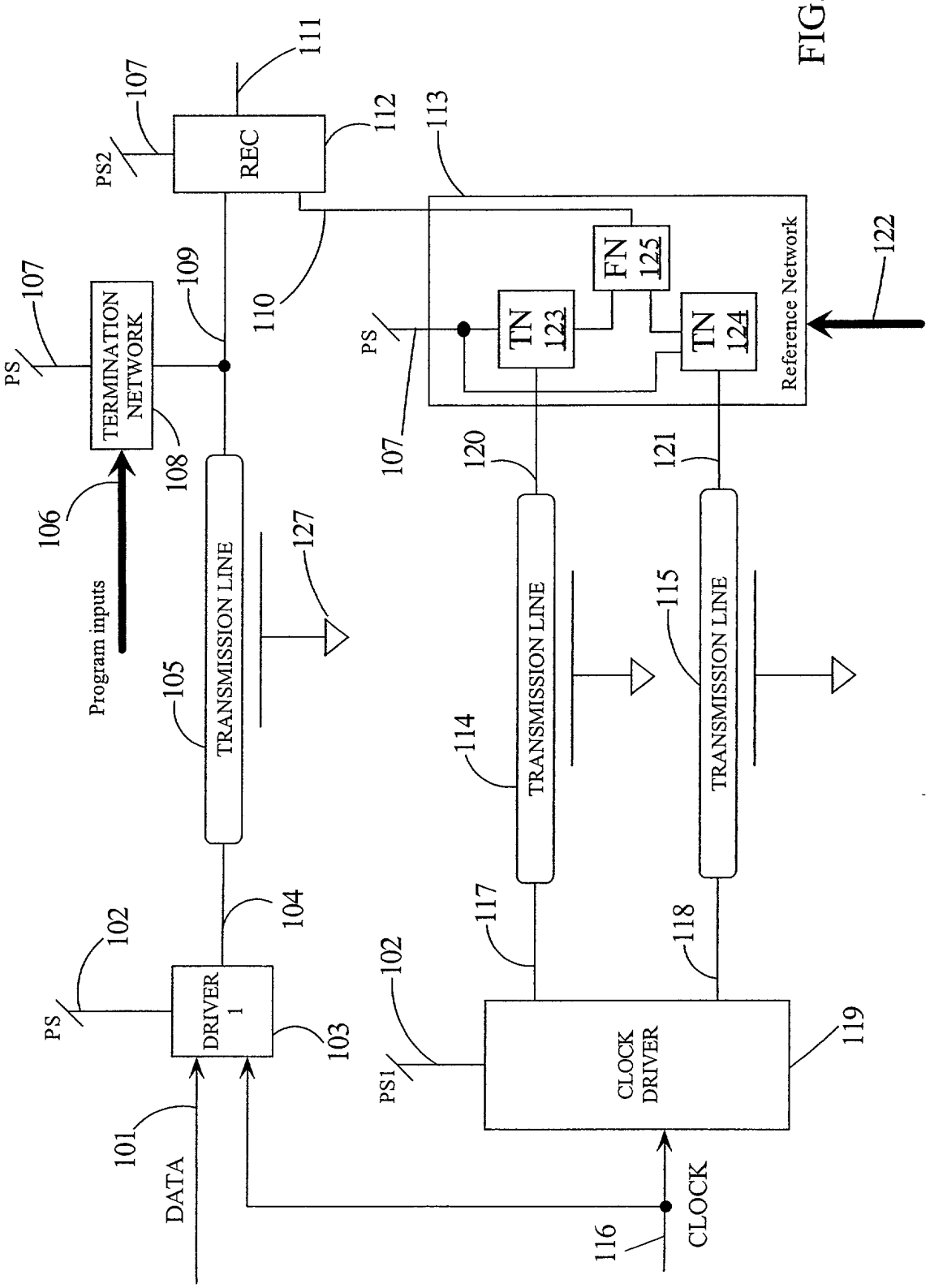



FIG. 1

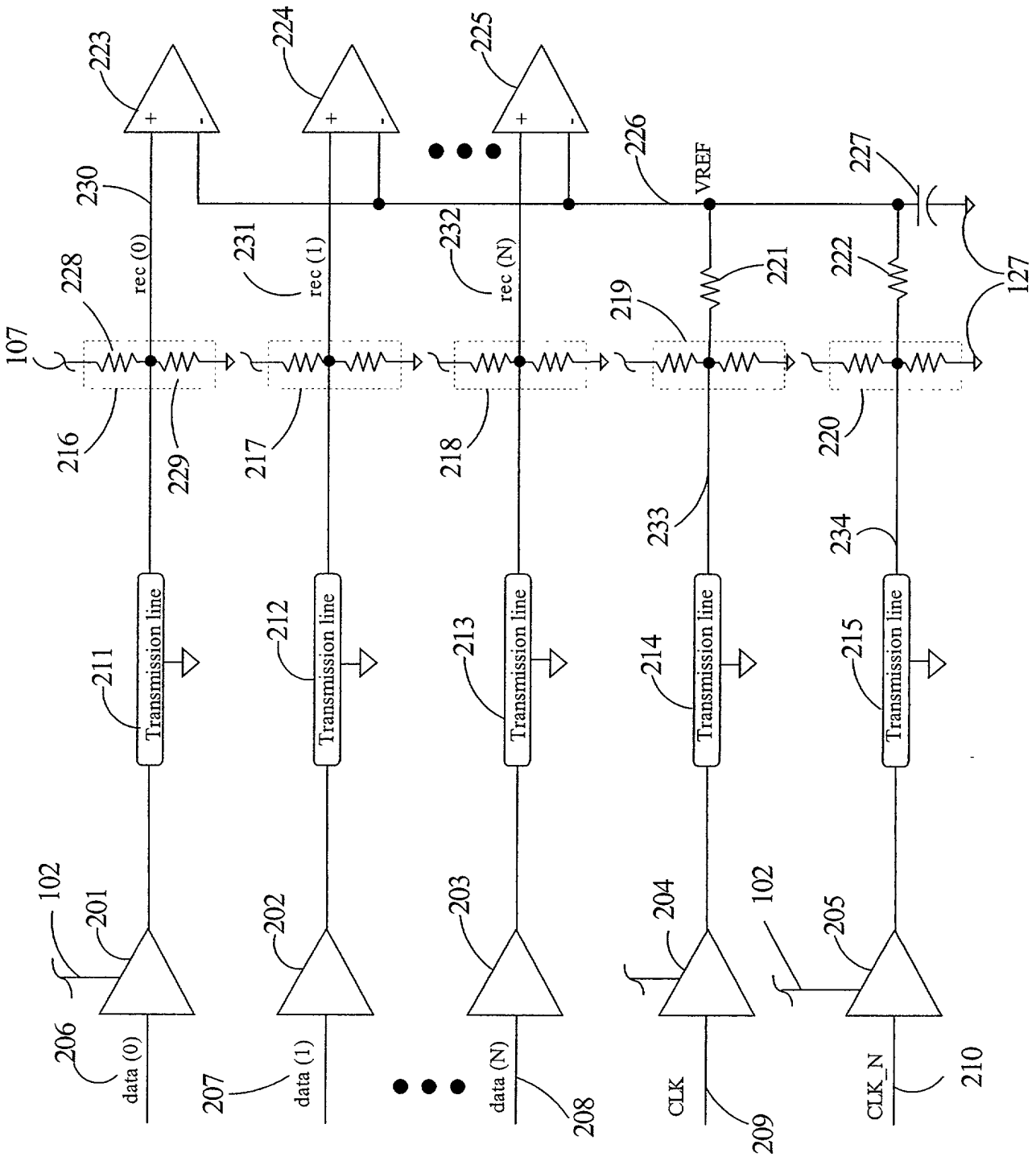
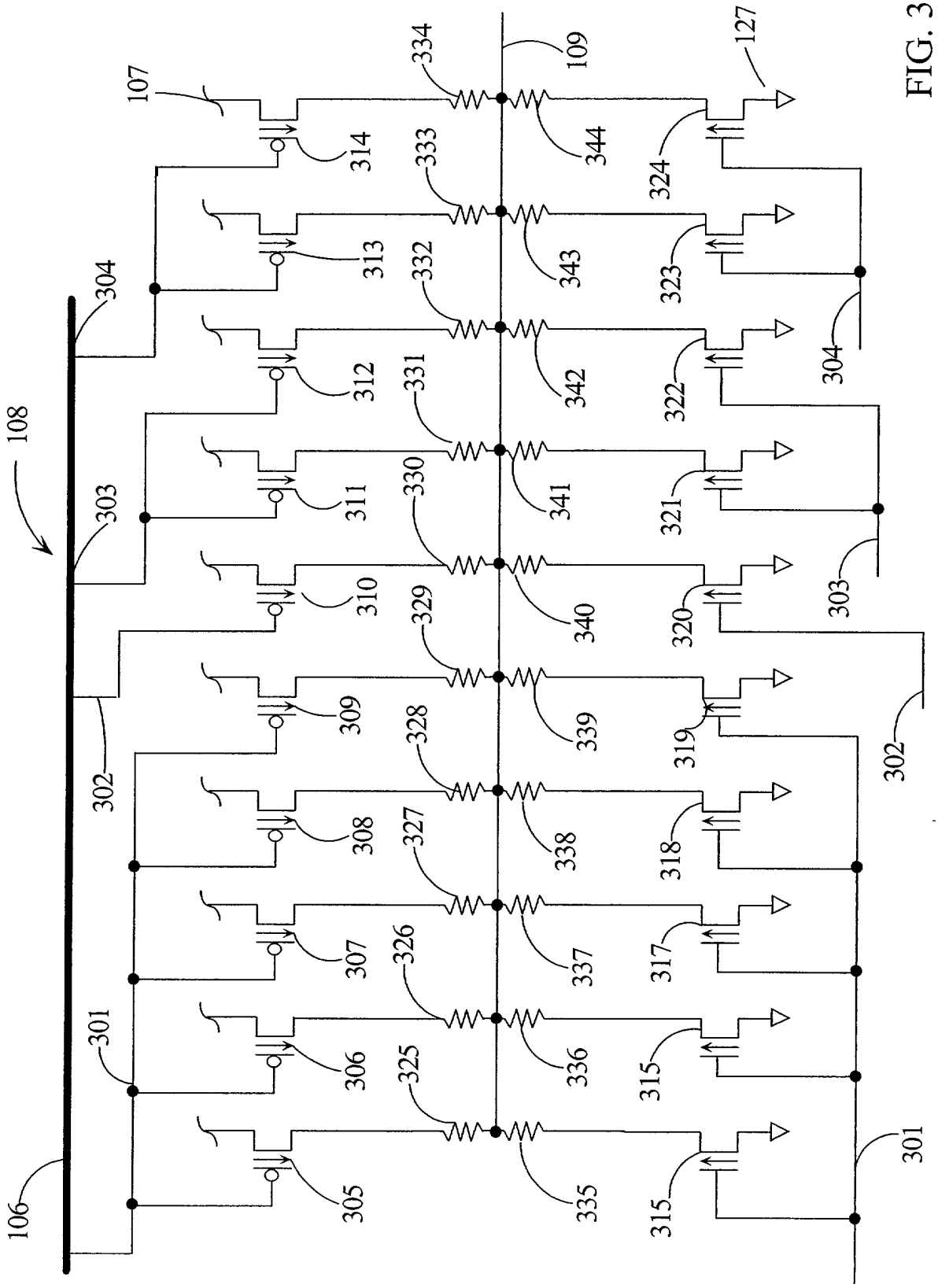

223
224
225
230
231
232
226
VREF
227
228
rec (0)
rec (1)
rec (N)
219
221
222
127
107
216
229
217
218
220
233
234
Transmission line
211
212
213
214
215
102
201
202
203
204
205
206
207
208
209
210
data (0)
data (1)
data (N)
CLK
CLK_N

FIG. 2


106
108
107
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127
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302
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FIG. 3

No. of parallel resistors 402 | Logic states of program signals 403

| UP | DOWN | P1 301 | P2 302 | P3 303 | P4 304 |
|---|---|---|---|---|---|
| 5 | 5 | 1 | 0 | 0 | 0 |
| 6 | 4 | 0 | 0 | 1 | 1 |
| 4 | 6 | 1 | 1 | 0 | 0 |
| 7 | 3 | 0 | 1 | 0 | 1 |
| 3 | 7 | 1 | 0 | 1 | 0 |
| 8 | 2 | 0 | 0 | 0 | 1 |
| 2 | 8 | 1 | 1 | 1 | 0 |
| 9 | 1 | 0 | 1 | 0 | 0 |
| 1 | 9 | 1 | 0 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 | 0 |
| 0 | 10 | 1 | 1 | 1 | 1 |

401

405 Results using 500 Ω resistors | 404 Source resistance of Terminating network | 403 Logic states of program signals

| UP | DOWN | $Z_T$ | P1 301 | P2 302 | P3 303 | P4 304 |
|---|---|---|---|---|---|---|
| 100 Ω | 100 Ω | 100 Ω//100 Ω=50 Ω | 1 | 0 | 0 | 0 |
| 83 Ω | 125 Ω | 83 Ω//125 Ω=50 Ω | 0 | 0 | 1 | 1 |
| 125 Ω | 83 Ω | 125 Ω//83 Ω=50 Ω | 1 | 1 | 0 | 0 |
| 71 Ω | 166 Ω | 71 Ω//166 Ω=50 Ω | 0 | 1 | 0 | 1 |
| 166 Ω | 71 Ω | 166 Ω//71 Ω=50 Ω | 1 | 0 | 1 | 0 |
| 62.5 Ω | 250 Ω | 62.5 Ω//250 Ω=50 Ω | 0 | 0 | 0 | 1 |
| 250 Ω | 62.5 Ω | 250 Ω//62.5 Ω=50 Ω | 1 | 1 | 1 | 0 |
| 55.5 Ω | 500 Ω | 55.5 Ω//500 Ω=50 Ω | 0 | 1 | 0 | 0 |
| 500 Ω | 55.5 Ω | 500 Ω//55.5 Ω=50 Ω | 1 | 0 | 1 | 1 |
| 50 Ω | ∞ | 50 Ω//∞ Ω=50 Ω | 0 | 0 | 0 | 0 |
| ∞ | 50 Ω | ∞//50 Ω Ω=50 Ω | 1 | 1 | 1 | 1 |

402

FIG. 4

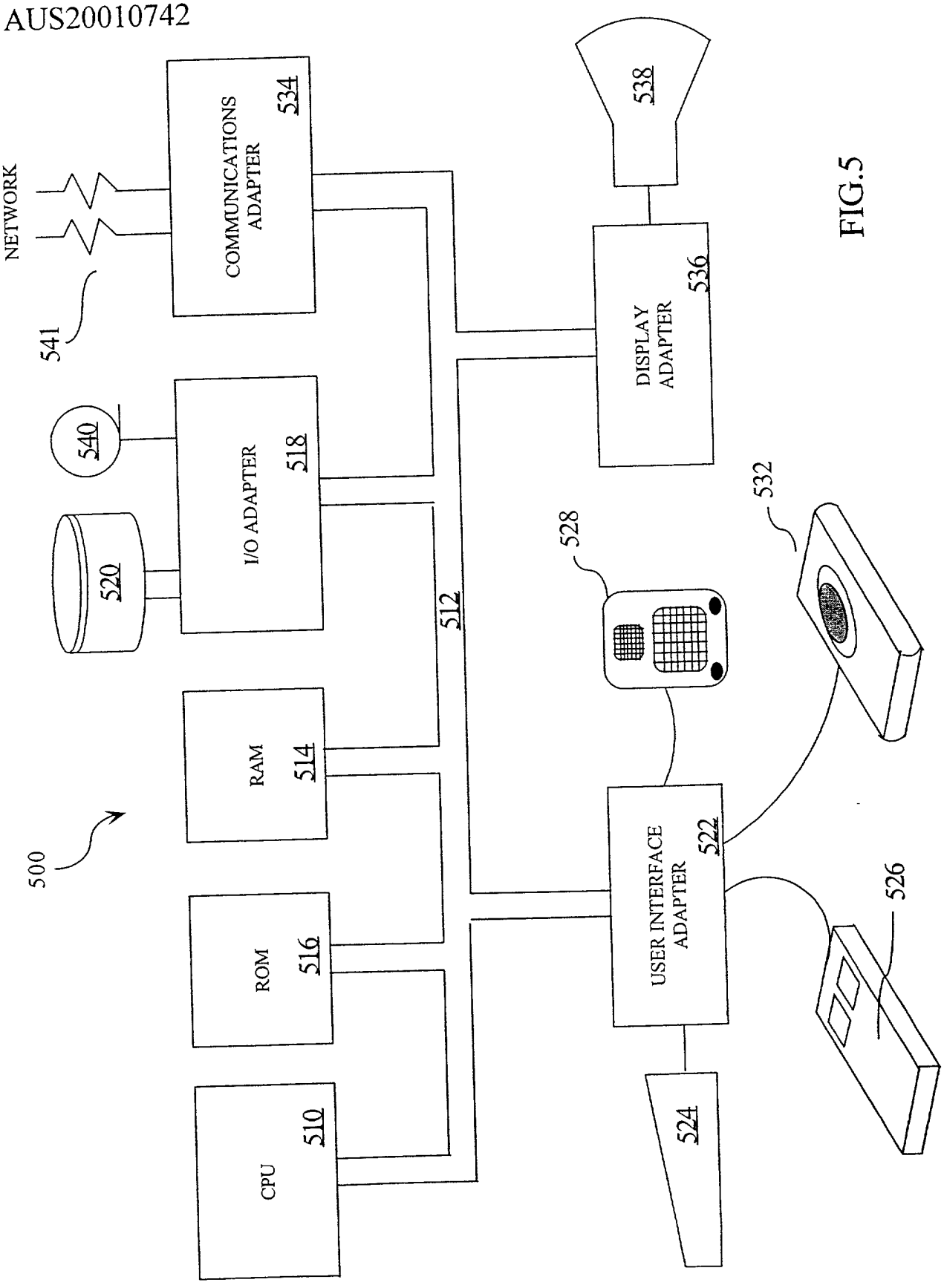
NETWORK
541
COMMUNICATIONS ADAPTER
534
538
DISPLAY ADAPTER
536
540
I/O ADAPTER
518
520
512
528
532
RAM
514
500
ROM
516
USER INTERFACE ADAPTER
522
526
CPU
510
524

FIG.5